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10/749,831	12/30/2003	Kevin M. Conley	SNDK.247US0	9380

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,831	CONLEY ET AL.	
	Examiner	Art Unit	
	CRAIG E. WALTER	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4 and 26-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4 and 26-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :10/29/07;11/1/07;12/18/07;2/4/08;2/13/08.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11 November 2007 has been entered.

Status of Claims

2. Claims 2-4 and 26-40 are pending in the Application.

Claims 1 and 5-25 remain cancelled.

Claims 36-40 are new.

Claims 2-4 and 26-40 are rejected.

Response to Amendment

3. Applicant's amendments and arguments 11 November 2007 filed on in response to the office action mailed on 21 June 2007 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Information Disclosure Statement

4. The five information disclosure statements (IDS) submitted on 29 October 2007, 1 November 2007, 18 December 2007, 4 February 2008, and 13 February 2008 were fully considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 2-4, 28-30 and 36-40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

More specifically, claim 2 recites "a pre-set proportion of the given number", however Examiner is unable to locate support in the original specification for a pre-set proportion of a given number of units of data as being used to determine if and when data is stored in a first, or second data block. Certainly Applicant's original specification supports using "a proportion" of the given number to make this determination, however the question remains if that proportion is determined ahead of time (e.g. pre-set). Examiner contends that that support is not present. A similar rejection applies to claims

28, 36 and 40, for "pre-set fraction", “pre-set fraction", and “pre-determined fraction” respectively.

Claims 3, 4, 29, 30, and 37-39 are rejected for further inheriting the deficiencies of each of their respective base claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2-4, 28, 29, 31, 32, 34, 36, 38 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US PG Publication 2002/0099904 A1).

As for claim 2, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

responding to a plurality of successive host commands to write a number of units of data that individually have sequential logical addresses less than a pre-set proportion of the given number by writing their data into a first designated block, and responding to host commands to write a number units of data having sequential logical addresses equal to or in excess of the pre-set proportion of said given proportion of said given number by writing their data into a block other than the first designated block (paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the

amount of data to be stored is equal to or less than/greater than the capacity of the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate Conley as physically storing data in a sequential manner (i.e. contiguous pages)).

To help illustrate this point, assume *arguendo*, that "a number of units of data" (hereinafter given number) is equal to the storage capacity of one of Conley's entire blocks, and that "a pre-set proportion" equals 100% of said given number. Conley's system, determines that a number of writes equal to or greater than said given number could not be written to a partial written block (e.g. first designated block), hence the data would be written to a block other than the first designated block. Also, if the amount of data to be written is less than 100% the capacity of a full block, and there is enough space to write that amount of data to a partially written block, Conley would write that number of units less than 100% of said given number to a partially written block (e.g. first designated block) in accordance with the flow illustrated in Fig. 14 of Conley.

As for claim 28, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

dedicating at least a first one of the blocks to store a number of units of data having sequential logical addresses less than a pre-set fraction of said given number

(as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block).

responding to a plurality of host commands to individually write units of data into the memory system by determining whether a number of the units of data with sequential logical addresses is less than the pre-set fraction, and, if so, by writing the data into the first designated block, and responding to host commands to write units of data having a number of sequential logical addresses equal to or in excess of the pre-set fraction of said given number by writing the data into a block other than the first dedicated block (paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the amount of data to be stored is equal to or less than/greater than the capacity of the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate Conley as physically storing data in a sequential manner (i.e. contiguous pages)).

To help illustrate this point, assume *arguendo*, that “a number of units of data" is equal to the storage capacity of one of Conley's entire blocks, and that "a pre-set fraction" equals 100% of said given number. Conley’s system, determines that a number of writes equal to or greater than said given number could not be written to a partial written block (e.g. first designated block), hence the data would be written to a block other than the first designated block. Also, if the amount of data to be written is less than 100% the capacity of a full block, and there is enough space to write that

amount of data to a partially written block, Conley would write that number of units less than 100% of said given number to a partially written block (e.g. first designated block) in accordance with the flow illustrated in Fig. 14 of Conley.

As for claim 31, Conley teaches a method of operating a non-volatile memory system in response to commands received from a host to individually write logically addressed units of data therein, the memory system having memory cells grouped into blocks that are simultaneously erasable and which individually store a given number of units of data at individual physical addresses, the logical addresses of received units of data being mapped within the memory system into corresponding physical addresses where the received units of data are stored, comprising:

allocating a first one of the blocks to store units of data having a number of sequential logical addresses less than a fraction of said given number (Fig. 14, elements 52, 53, 61, 63 – paragraph 0062 – if the system determines that enough space is available to accommodate the amount of data required by the pages corresponding to a number of logical addresses, the data will be allocated to the partially written block) ,

allocating a second one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number (Fig. 14, elements 52, 53, 55 – paragraph 0062 – if the system determines if a sufficient amount of space is not available to accommodate the amount of data required by the pages corresponding to the number of logical addresses, a second block (new erased block) will be allocated to store the data),

in response to receipt of a command to write data having a number of sequential logical addresses less than said fraction, determining whether the first block has sufficient erased capacity to store the received data and, if so, writing the received data into sequential physical addresses of the first block (Fig. 14, elements 61 and 67 – paragraph 0062 – once the system determines that enough pages are available in the partially written block (i.e. element 61), the data will be written into the newly allocated block (element 67)), and

in response to receipt of a command to write data having a number of sequential logical addresses equal to or in excess of said fraction, determining whether the second block has erased capacity to store the data and, if so, writing the data into sequential physical addresses of the second block (Fig. 14, elements 55 and 57 – paragraph 0062 – once the system determines that a new erased block is sufficient to store the data, the new data is written to the block (element 57)).

As for claim 32, Conley teaches,

in response to receipt of the command to write data having a number of sequential logical addresses less than said fraction, if the first block does not have sufficient erased capacity to store the received data, allocating a third one of the blocks to store units of data having a number of sequential logical addresses less than a fraction of said given number and then writing the received data into sequential physical addresses of the third block (Fig. 14, elements 65 and 67 – paragraph 0062 – once the system determines that the partial block is not large enough, a new erased block (third) will be allocated and written to), and

in response to receipt of the command to write data having a number of sequential logical addresses equal to or in excess of said fraction, if the second block does not have sufficient erased capacity to store the received data, allocating a fourth one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number and then writing the received data into sequential physical addresses of the fourth block (Fig. 14, elements 55 and 57 – paragraph 0062 – once the system determines that a one new erased block is not sufficient to store the data, an additional block (i.e. fourth) will be allocated to accommodate the new data (elements 55 and 57)).

As for claim 3, Conley teaches determining whether or not the successive host commands individually include a number of units of data having sequential logical addresses less than the pre-set proportion of said given number (referring again to paragraph 0062, and the rejections stated above, the given number is based on the size of an entire block).

As for claims 4, 29 and 34, Conley teaches the non-volatile memory cells as being organized into multiple sub-arrays, and said blocks of memory cells include memory cells of two or more of the sub-arrays (paragraph 0062, all lines, if the amount of host data does not exceed the size of one full block the data, two different sets of host writes can be stored uniquely in one block (i.e. each write is a unique sub-array of data within each block). Also note Conley specifically teaches his memory system as including sub-arrays in paragraph 0010, lines 1-7).

As for claim 36, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

designating at least a first one of the blocks to store a number of units of data received by the memory system with individual ones of multiple write commands that have sequential logical addresses less than a pre-set fraction of said given number (as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block),

responding to the receipt of multiple commands by the memory system to individually write one or more units of data thereinto by, for individual commands (data is written to the memory in accordance with the host's commands),

(a) determining whether the command specifies the writing of a number of units of data having sequential logical addresses that is less than the pre-set fraction (paragraph 0062, all lines – the system determines the amount of data to write), and (b) determining whether the first block has enough erased capacity to store the number of units of data provided with the command (figure 14, partial blocks are checked to determine if enough capacity is available to store the data before data is either stored in partial block, or to a new one/s), wherein

when both of conditions (a) and (b) above are determined to exist, thereafter writing the units of data into the first block (paragraph 0062, all lines –

if less than a full block is to be written, and there is enough space in the partially written block, the data will be written to the partially written block), but

when either one of conditions (a) or (b) above is determined not to exist, writing the units of data into one of the blocks other than the first block (if more data than one the size of one block is to be written or the partial block lacks the capacity to store the entire set of data is written to the new block – figure 14).

As for claim 38, Conley teaches:

designating at least a second one of the blocks to store a number of units of data received by the memory system with individual ones of multiple write commands that have sequential logical addresses equal to or greater than the pre-set fraction (figure 14, element 55, the newly addressed block will store the data), and

responding to the receipt of multiple commands by the memory system to individually write one or more units of data thereinto by additionally, for individual commands (the system will follow the flow illustrated in Fig. 14 for the commands transmitted by the host),

(c) determining whether the command specifies the writing of a number of units of data greater than the given number (Fig. 14, element 53), wherein when neither of the conditions (a) nor (c) above exist, writing the units of data into the second block, without regard to whether condition (b) exists or not, but when the condition (c) above is determined to exist, writing the units of data into one of the

blocks other than the first or second blocks (again, (if more data than one the size of one block is to be written or the partial block lacks the capacity to store the entire set of data is written to the new block – Fig. 14).

As for claim 40, Conley teaches a non-volatile memory system having memory cells grouped into blocks that are simultaneously erasable and which individually store a given number of units of data at individual physical addresses, the logical addresses of received units of data being mapped within the memory system into corresponding physical addresses where the received units of data are stored, a method of operation in response to received commands to individually write logically addressed units of data therein, comprising:

designating a first one of the blocks to store units of data having a number of sequential logical addresses less than a pre-determined fraction of said given number (as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block),

designating a second one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number (newly addressed block – Fig. 14, element 55),

providing at least another one of the blocks that is fully erased (Fig. 14, element 57, a block or multiple blocks will be provided depending on the size of the data), and

in response to receipt of a command to write data into the memory system, identifying the number of units of the data that have sequential logical addresses,

determine whether the number of such units with sequential logical addresses are less than the fraction (Fig. 14, element 53), and, if so,

writing the data to the first of the blocks (if enough capacity exists in the partially written block, the data will be written in the partial block), but if the amount of data is not less than the fraction, then

writing the data to the second of the blocks if there is sufficient capacity therein, but if there is not sufficient capacity in the second of the blocks, writing the data to the fully erased block (if the partially written block does not have enough space the data will be first written to a newly addressed block, and additional blocks if the additional capacity is required 0 Fig. 14, elements 53, 55, and 57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 26, 27, 30, 33, 35, 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (US PG Publication 2002/0099904 A1) as applied to claims 2 and 28 above, and in further view of Kulkarni et al. (Us PG Publication 2002/0034105 A1), hereinafter Kulkarni.

As for claims 26, 27, 30, 33, 35, 37 and 39, though Conley teaches all the limitations of claims 2 and 28, he fails to specifically teach the pre-set proportion as being set within a range of 25-75 percent of the given number as recited by Applicant in these claims.

Kulkarni however teaches a system and method for incrementally updating an image in flash memory wherein new flash images are built incrementally until a memory block is of sufficient size to be written to the flash memory – paragraph 0013, all lines. More specifically, Kulkarni teaches writing memory to a first memory block (i.e. RAM), until the memory is half full (i.e. 50 percent), and subsequently writing the data to a second block in the flash memory (i.e. predetermined limit set at 50% allocation) – paragraph 0014, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Conley to further include Kulkarni's system for updating an image in flash memory into his own system for partial block data programming in a non-volatile memory. By doing so, Conley would have a more efficient memory system capable for reducing the number of sections transmitted during the writing process, while persevering sections that are used to construct other section as taught by Kulkarni in paragraph 0011, all lines. Additionally, Conley could benefit from Kulkarni's system by preventing the problems related to data overwrite as described by Kulkarni in paragraph 0012, all lines.

Response to Arguments

8. Applicant's amendments and arguments with respect to the claims rejected under the 35 USC §§ 102(b) and 103(a) have been fully considered, but they are not persuasive (e.g. claims 2-4, 28 and 29).

Under the heading, "Claims 2-4, 26 and 27", Applicant contends (in light of the new amendments to the claims), "[e]ven if it is argued that Conley has a pre-set proportion of the capacity of a partially written block available for storage of additional data, that proportion will vary from partially written block to partially written block. Conley does not suggest writing quantities of data less than the defined pre-set proportion from a plurality of successive host commands into a designated block. The concern in Conley is to match the amount of data to be written with the erased storage capacity of the blocks" (page 9 of remarks, ll. 9-15).

This argument however is not persuasive. Examiner maintains that not only does Conley teach a constant, pre-set proportion, but that Conley additionally teaches only writing to the first block if the amount of data associated with the host's commands is less than that pre-set proportion of a given number. To help illustrate this point, assume *arguendo*, that "a number of units of data" is equal to the storage capacity of one of Conley's entire blocks, and that "a pre-set proportion" equals 100% of said given number. Conley's system, determines that a number of writes equal to or greater than said given number could not be written to a partial written block (e.g. first designated block), hence the data would be written to a block other than the first designated block. Also, if the amount of data to be written is less than 100% the capacity of a full block,

and there is enough space to write that amount of data to a partially written block, Conley would write that number of units less than 100% of said given number to a partially written block (e.g. first designated block) in accordance with the flow illustrated in Fig. 14 of Conley.

Continuing on page 9, ll. 19-24 (with respect to claim 3), Applicant argues, "[even if it is argued that Conley has a pre-set proportion of the capacity of a partially written block available for storage of additional data, Conley does not suggest determining whether successive commands contain a number of units of data with a number of sequential logical addresses that is less that the stated threshold."

This argument however is not persuasive. Again, Conley's system examines successive commands, and determines if the amount of data to be written to the partial blocks exceeds the capacity for that particular block to store the data associated with the command/s. If the first (i.e. partial) block has sufficient capacity, the data will be written to that block, else a new block or new blocks will be allocated to satisfy those command/s – Fig. 14, elements 53, 55 and 57.

As for dependant claims 26 and 27, Applicant asserts, "it is not seen how Conley could use any fixed threshold data amount to make decisions on how to direct data writes, since this clearly depends on the storage capacity of available blocks which will vary. The adoption of Kulkarni's percentage limit in Conley appears to have been non-obvious for that reason… The percentage threshold of Kulkarni is used to decide *when* to write data into the memory, not to direct *where* the data are to be written, as is the case with claims 26 and 27 (emphasis added by Applicant, page 10, ll. 1-9).

These arguments however are not persuasive. The latter argument (alleging that Kulkarni is used to decide when, not where to write data) is not persuasive as it fails to address Conley and Kulkarni's teachings in combination. The question of obviousness is not determined by what one of the references relied upon teaches, but rather if the combination of those teachings in fact render the invention as a whole, obvious (see MPEP § 2141.02 I.). The former argument does in fact allege that the combination of the teachings fail to render the invention non-obvious, however the justification provided to support this allegation is not persuasive. More specifically, Examiner maintains that it would have been obvious for Conley to impose a 50% allocation limit of data blocks into his system for writing to partial blocks, and that such a limit doesn't necessarily preclude Conley's system from continuing to function on blocks whose capacity may vary dynamically, Applicant's arguments notwithstanding. Such a system would still determine whether to write to a first partially written block, or to allocate a new block in accordance to the flow chart illustrated in Fig. 14. The difference is that rather than Conley writing partial block up to, but not beyond, its capacity; the block would be written to the 50% allocation limit. Kulkami demonstrates latter as in fact being obvious, and Examiner maintains that an artisan of ordinary skill would be motivated to do combine Conley with Kulkami based on the reasoning explicitly extracted from Kulkarni's teaching reference, restated in the § 103(a) rejection set forth *supra*.

Applicant's arguments under the heading "Claims 28-30" are substantially similar to those set forth under the preceding heading in Applicant's remarks, hence they are

not persuasive for the same reasons as discussed in Examiner's retort to Applicant's remarks under that heading.

Under the heading, "Claims 31-35", Applicant asserts that Conley fails to teach, "determining whether the number of units of data are above or below the specified threshold that is set with respect to two allocated blocks… [and that Conley] does not suggest allocating first and second blocks for storage of a number of units of data in one or the other of these blocks depending whether the amount of data is above or below the specified threshold" (remarks, page 11, l. 23 through page 12, l. 1).

These arguments however are not persuasive. The point of contention between Applicant and Examiner appears to be whether or not Conley teaches determining where to store data based on a pre-set or pre-determined threshold. As clearly stated in the rejection of claim 31, *supra;* assume *arguendo*, in which "a number of units of data" is equal to the storage capacity of one of Conley's entire blocks, and that "a pre-set proportion" equals 100% of said given number. Conley's system, upon determining that a number of writes equal to or greater than said given number, could not be written to a partial written block (e.g. first designated block), hence the data would be written to a block other than the first designated block. Also, if the amount of data to be written is less than 100% the capacity of a full block, and there is enough space to write that amount of data to a partially written block, Conley would write that number of units less than 100% of said given number to a partially written block (e.g. first designated block) in accordance with the flow illustrated in Fig. 14 of Conley.

Continuing under this heading (page 12, ll. 9-11), Applicant's argument of Conley being silent with respect to the "second positive limitation" that checks the amount of data against the fraction of the block storage capacity is not persuasive. Examiner maintains that based on the "broadest reasonable interpretation consistent with [Applicant's] specification" pursuant to MPEP § 2111, the fraction of the capacity can be the entire capacity itself. Based on this assumption, the "second positive limitation" as characterized by Applicant is in fact inherent to a system such of Conley's; since this comparison would occur during step 53 of Fig. 14 when determining if sufficient capacity of the partial block exists.

Under the heading, "New Claims", Applicant contends that these new claims (e.g. 36-40) were drafted to recite features of other pending base claims (e.g. claims 2 and 31) which allegedly are novel over Conley's disclosure. These arguments however are not persuasive for the reasons set forth in Examiner's response to arguments above.

Applicant arguments with respect to the newly added claims are not persuasive, as Examiner maintains that Conley renders each of these claims either anticipated and/or obvious as per the rejections and arguments presented *supra*.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Craig E Walter/
Examiner, Art Unit 2188

CEW

/Hyung S SOUGH/
Supervisory Patent Examiner, Art Unit 2188